GUIDELINE TO THE OPERATION OF EMI EMISSION REDUCTION OF CH7017/CH7019

1. Introduction

CH7017/CH7019 provides a capability to reduce the EMI emission from LVDS output paths by software control. The method is by controlling the CH7017/CH7019 LVDS PLL registers settings, the LVDS output clock spectrum can be spread (up to 2.5%) and the energy of the peak of the spectrum is reduced, that the EMI emission is therefore reduced.

2. Registers Settings for EMI Emission Reduction (ER) Operation

The registers settings involved in this operation are divided into two parts: (1) Basic registers settings; (2) Clock dependent registers settings. They are described below.

2.1 Basic register settings to activate the ER operation

In order to turn on ER operation, the registers shown on **Table 1** should be set to the specified values independent of the operating frequency.

Table 1: The basic registers settings to turn on the ER operation

Symbol	Register	Setting	Remarks
ER On/Off	7Dh[4:2]	111	Turn on EMI emission reduction operation
Ref clock	70H[4:3]	01	Reference clock input
SS divider	70H[6:5] 71H[6] 70H[7]	11 0 1	Value for SS divider
CP Current	73h[2:0]	000	Charge pump current (=72uA)
LP resistor	76h[6:4]	010	Loop resistor (=1000ohm)
LP capacitor	78h[6:5]	00	Loop capacitor (=100pF)
VCO unit	72h[3:0]	1101	3.3unit
Oscillator Current	75h[2:0]	100	Oscillator Current (=40uA)
PLLCAP	----	0.1nF	Connected externally from CH7017/7019 pin 2 to Ground with 0.1 nF capacitor

2.2 Clock dependent registers settings

Table 2 shows the clock dependent ER registers settings.

Table 2: Clock dependent registers settings for different % of frequency spreading

Operating frequency (MHz)	LPSSFD 7Ah[2:0]+7Bh[7:0]	LPSSFB 70h[2:0]+6Fh[7:0]	LPSSFF 7Dh[7:5]+7Eh[7:0]	SS ±0.5%~1% 75h[6:3]	SS ±1%~2% 75h[6:3]	SS ±2%~3% 75h[6:3]
40	100+00011101	000+00010011	000+00010011	1010	0001	1111
65	101+00111101	000+00100111	000+00100111	1010	0001	1101
108*	011+01001001	000+00011011	000+00011011	1010	1001	1111
162*	100+00110101	000+00110011	000+00110011	1100	1010	0001

* When the operating frequency is higher than 100MHz, LVDS operates in dual channel mode.

If the ER function is to be turned off, change ER ON/OFF bits 7Dh[4:2] (see **Table 1**) to {000}, and set LPSSFB and LPSSFF bits to all 0's.

3. Measured Spectra

Figure 1 shows the spectrum without ER operation at the operating frequency 65 MHz.

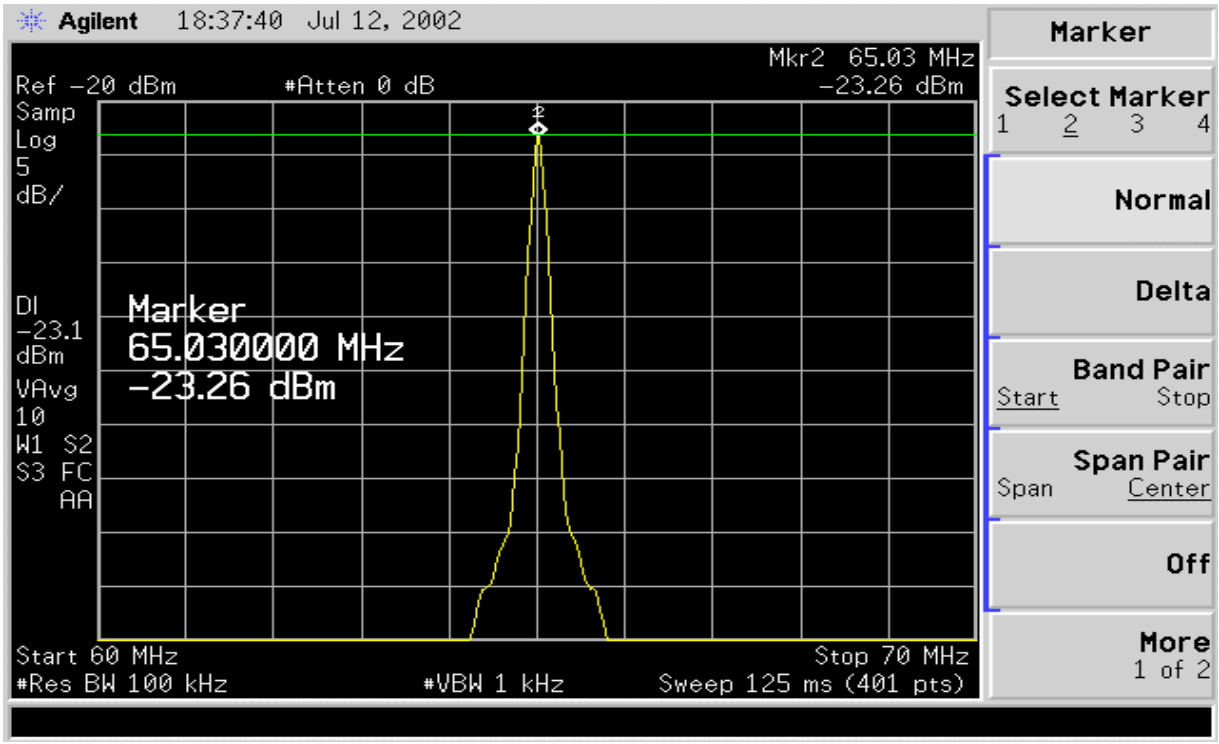

Figure 1: EMI emission reduction operation off

Figures 2 shows the spectrum with ER operation turned on for 0.75% spreading at the operating frequency 65 MHz.

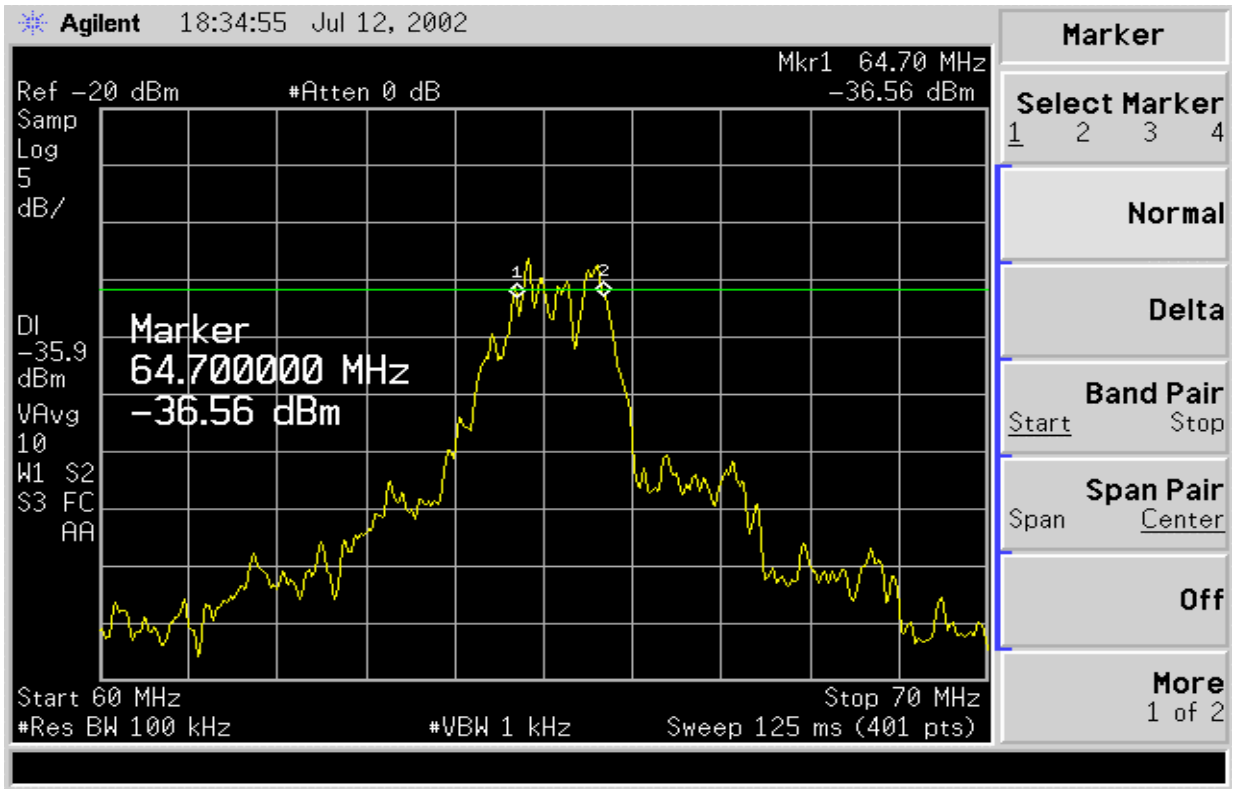

Figure 2: EMI emission reduction operation 0.75% clock spreading

Figures 3 shows the spectrum with ER operation turned on for 1.5% spreading at the operating frequency 65 MHz.

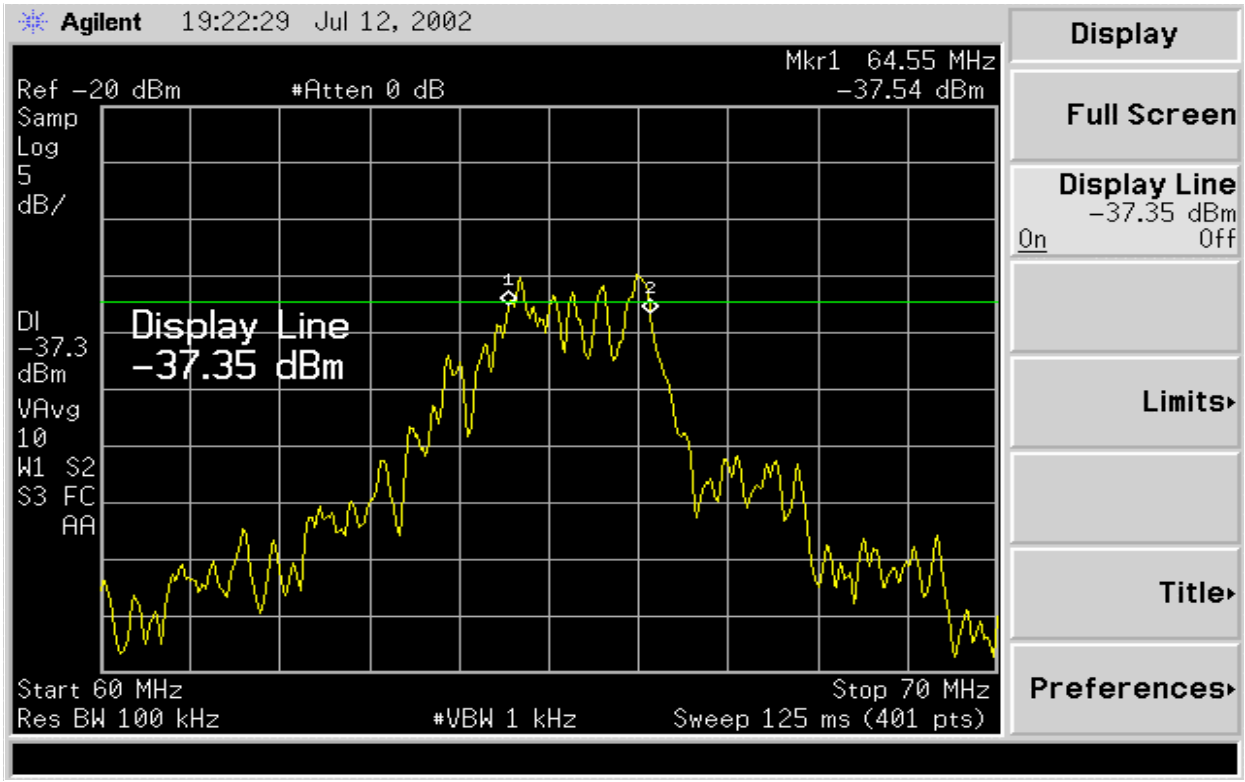

Figure 3: EMI emission reduction operation 1.5% clock spreading

Figures 4 shows the spectrum with ER operation turned on for 2.5% spreading at the operating frequency 65 MHz.

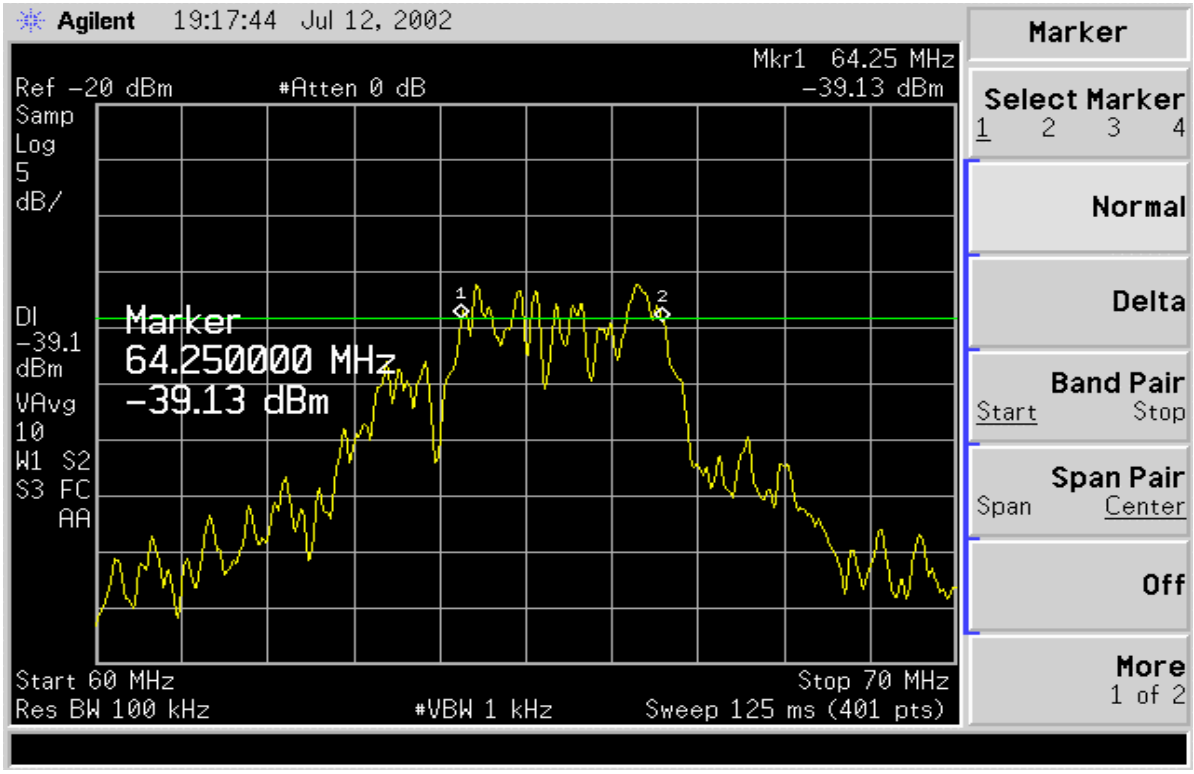

Figure 4: EMI emission reduction operation 2.5% clock spreading

4. Summary of the Panels Tested

The LVDS panels tested with the EMI emission reduction operation are listed in **Table 3**.

Table 3: The list of panels tested with ER Operation

Maker	Model #	Resolution	Test Result	Remarks
QDI	141X1LH02	XGA 1024x768	Passed with 0.75% spreading	The panel has narrow Hsync tolerance and is not able to accept clock with the spreading of either 1.5% or 2.5%.
LG.Philips	LP141X8 (A1C2)	XGA 1024x768	Passed with 2.5%	
LG.Philips	LP150X2 (A2C4)	XGA 1024x768	Passed with 2.5%	
Samsung	LTN141XD-L01	XGA 1024x768	Passed with 2.5%	
Samsung	LTN150XD-L01	XGA 1024x768	Passed with 2.5%	